Sub-threshold Logic for Ultra-Low Power Consumption

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Abstract-- **In the ultra low power end of design spectrum when performance is of secondary importance, digital subthreshold logic circuits are more applicable than the regular MOS logic. In this paper, we propose two different subthreshold logic families: 1) variable threshold voltage subthreshold CMOS (VT-Sub-CMOS) and 2) subthreshold dynamic threshold voltage MOS (Sub-DTMOS) logic. Both these logic families have comparable power consumption as regular subthreshold CMOS logic along with superior robustness and tolerance to process and temperature variations.**

Keywords - Subthreshold logic; Sub-DTMOS; VT-Sub-CMOS.

I. INTRODUCTION

The continuous growth of recent mobile and portable devices and applications has caused a tremendous thrust for low power circuit design. Various methods and techniques, such as voltage scaling, clock gating, etc. have been applied successfully in the medium power, medium performance region of the design spectrum for lower power consumption. Nevertheless, in some applications where ultra-low power consumption is the primary requirement and performance is of secondary importance, a more aggressive approach is warranted. Operating the transistors of a digital logic in the subthreshold region has recently been proposed to achieve ultra-low power consumption. A subthreshold circuit has been shown to consume orders of magnitude less power than the regular strong-inversion circuit at the same operating frequency.

A subthreshold digital circuit manages to satisfy the ultra-low power requirement because it uses the leakage current as its operating switching current.

This minute leakage current, however, limits the maximum performance at which the subthreshold circuit can be operated. The subthreshold circuit is thus suitable for certain applications which do not require very high performance such as pace-makers and wearable wrist-watch computers. Subthreshold CMOS (Sub-CMOS) logic is the conventional CMOS logic operated in the subthreshold region. In order to ensure that the entire circuit is indeed operating in the subthreshold region, a power supply less than the threshold voltages of the transistors is used to power the circuit. In the subthreshold region, therefore, due to the absence of conducting inversion channels, transistors behave differently as compared to when they are operated in a normal strong inversion region. The rest of the paper is organized as follows : section 2 explains sub-CMOS logic (sub-threshold CMOS) with SAT scheme and discusses its merits and demerits. In section 3, we explain the properties and performance of sub-threshold DTMOS logic family, and compare them with regular subthreshold MOS logic circuits. Section 4 compares the stability of both logic families to the temperature and process variations. Finally, a conclusion is drawn in section 5.

II. VT-SUB-CMOS LOGIC

VT-Sub-CMOS logic is a sub-CMOS logic with an additional stabilization scheme (Fig.1). The stabilization circuit monitors any change in the transistor current due to temperature and process variations and provides an appropriate bias to the substrate. Any increase of the current above certain prespecified threshold value is thus reduced by an appropriate bias to the substrate. Both logic and stabilization circuits of VT-sub-CMOS work in the subthreshold region i.e., with a supply voltage less than the threshold voltage of the transistor.

There are two main components of the stabilization module in the VT-Sub-CMOS logic, namely, the leakage current monitor (LCM) and self-substrate bias (SSB) circuit (Fig. 2). LCM is used as a leakage current sensor and a control to the SSB circuit. It senses any fluctuation in the transistor current and activates the SSB circuit which then applies an appropriate bias to the substrate of the transistors. The circuit for LCM used in other cases works well for strong inversion operation but not in the subthreshold region of operation.

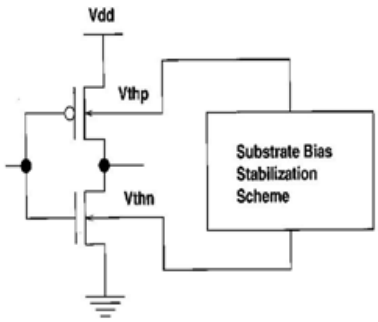

Figure 1. VT CMOS logic.

Leakage currents in PMOS and NMOS transistors are monitored separately. The conductivity of the sensor transistor in the LCM changes with temperature and process variations resulting in a change in output voltage, $V_{control}$. This change in the output voltage is detected and amplified by a buffer

circuit, which is used to activate the SSB circuit. Once activated, the SSB circuit then supplies a bias voltage to the substrate V_{bb} and restores the transistor conductivity back to its original value.

The SSB circuit contains a charge pump which is powered by pulses generated from a ring oscillator. The charge accumulated from the pump is used to bias the substrate of the transistors. The SSB circuit works intermittently and is activated by LCM whenever necessary. Once the required substrate bias is provided, the SSB circuit is deactivated by LCM. The LCM component thus acts as a thermostat which regulates the fluctuations due to temperature and process variations within a pre-specified tolerable range. The conventional charge pumps which are commonly used in Flash EPROM and EEPROM are used in the SSB circuit. The charge pump consists of diodes and associated charging capacitors. The charge pump should be strong enough to be able to drive the capacitive load by itself without any help from amplifying buffer. The buffer cannot be used to help drive the output of the charge pump because it will clip the output at V_{dd} and G_{nd},thus nullifying the effective output from the charge pump. In order to obtain better low-pass filtering and smoother output voltage, i.e., less "spiky" waveform, the charging capacitors can be made comparable to the load capacitor.

III. SUB- DTMOS LOGIC

DTMOS is a transistor whose gate is tied to its substrate (Fig.3). Thus, the substrate voltage in DTMOS changes with the gate input voltage, accordingly. Sub-DTMOS logic provides an alternative way to achieve the same stability with direct substrate biasing without using additional control circuitry as in the case of VT-sub-CMOS logic.

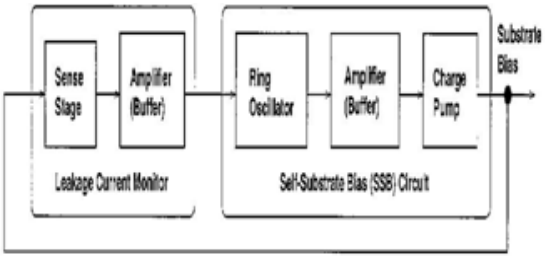

Figure 2. Components of the stabilization module.

Both dc and ac characteristics of Sub-DT-CMOS logic are analyzed and compared with those of Sub-CMOS logic. Results are obtained from SPICE simulations Figs. 4 and 5, respectively, show the delay and power consumption of inverter connected in a ring-oscillator fashion as a function of V_{dd}.

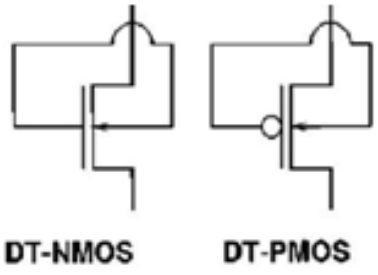

Figure 3. DT NMOS and DT PMOS

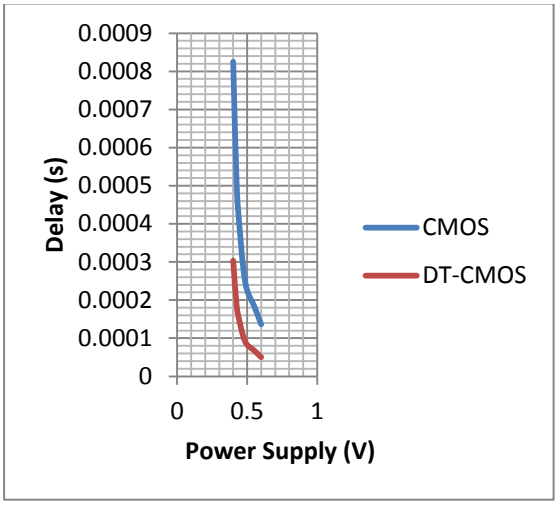

Figure 4. Delay Vs Vdd

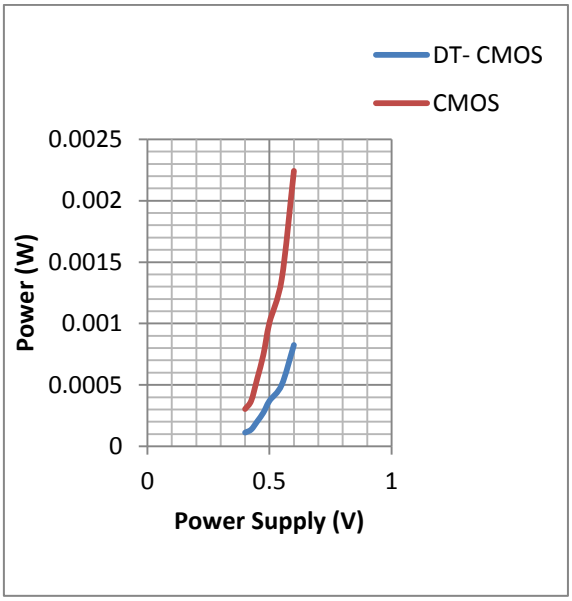

Figure 5. Power Vs Vdd.

The power-delay product (PDP) is a measure of the amount of energy/switching and can be used to determine whether the increase of power consumption is more dominant than the delay improvement, or vice-versa. Fig. 6 shows the PDP as a function of V_{dd} for both sub-DT-CMOS and sub-CMOS logic.

Sub-DT-CMOS logic can be operated at much higher switching frequency while maintaining the same energy/switching.

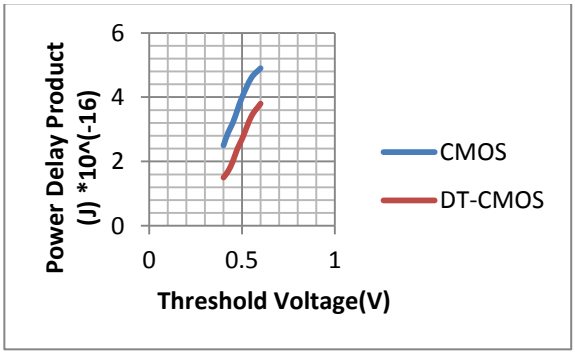

Figure 6. Power Delay Product Vs Vdd.

IV. RESULT

A. Temperature Variations

The effect of temperature variation is analyzed using SPICE simulation with $V_{dd} = 0.5$ V and the temperature parameter is being swept from room temperature 25℃ to 125℃.

At circuit level, the effect of temperature variation on the performance and energy/switching of regular sub-CMOS, VT-sub-CMOS, and sub-DT-CMOS logic are shown in Figs.7 and 8, respectively. As expected, both VT-sub-CMOS and sub-DT-CMOS logic are very effective in maintaining a stable operating frequency over the range of temperatures.

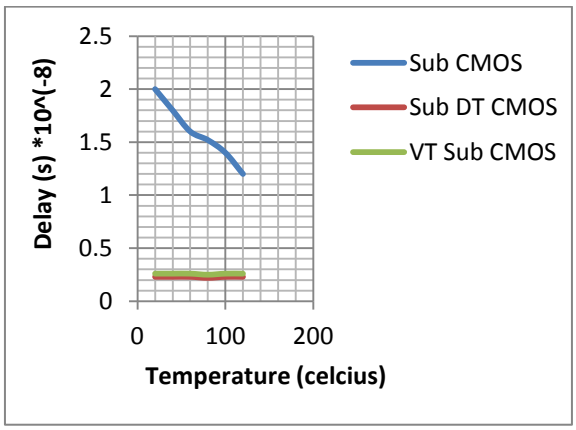

Figure 7. Delay Vs temperature.

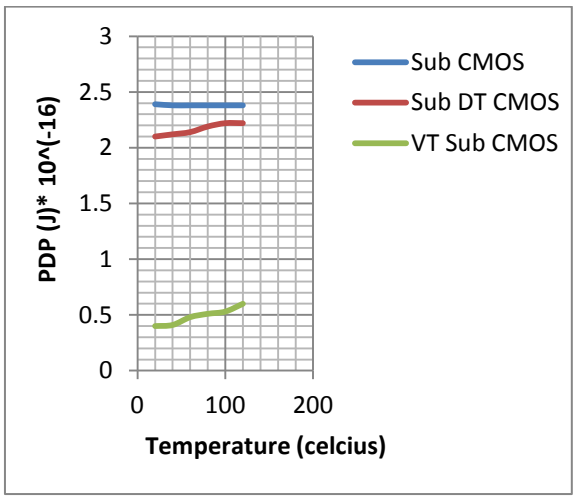

Figure 8. Power Delay Product Vs temperature.

B. Threshold Voltage Variations

The effect of process variations on sub-CMOS, VT-sub-CMOS, and sub-DT-CMOS logic are analyzed by varying the threshold voltages of both NMOS and PMOS by ±10% from their original designed values.

Figs. 9 and 10 show the delay and power-delay product, respectively, of sub-CMOS, VT-sub-CMOS, and sub-DT-CMOS logic. The inherent ro-bustness of sub-DT-CMOS and VT-sub-CMOS logic is again observed to be much higher than that of regular sub-CMOS logic.

To model the effects of process variations, we change the threshold voltages of the transistors in the SPICE model file, and to model the effects of temperature variations we simulate the circuit at both room temperature (25°C) and at 100℃.

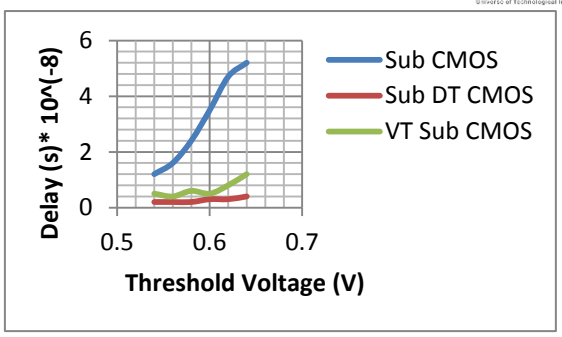

Figure 9. Delay Vs Threshold Voltage

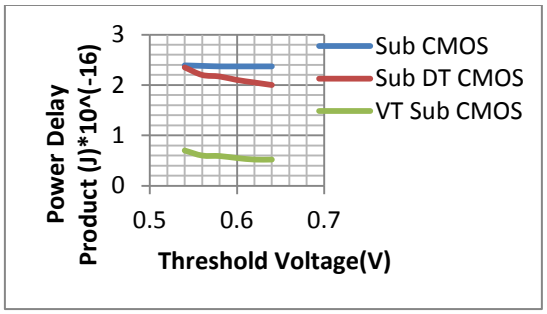

Figure 10. PDP Vs Threshold Voltage

V. CONCLUSION

In this paper, we discussed two novel subthreshold logic families. A new control circuit for the stabilization of subthreshold circuit is also discussed in detail. Both VT-sub-CMOS and sub-DTMOS logic families show superior robustness and tolerance to temperature and process variations than that of regular subthreshold CMOS logic. VT-sub-CMOS logic can be readily implemented in twin-well process technology, but it requires additional circuitry for stabilization. In contrast, sub-DTMOS logic does not require any additional stabilization circuitry but can only be implemented in triple-well process technology. The additional increase in area and process complexities for sub- DTMOS logic is compensated by its higher operating frequency while maintaining comparable energy/switching as regular subthreshold CMOS logic. DTMOS has been successfully implemented in both SOI and bulk Silicon. VT-sub-CMOS logic, however, has better control on substrate bias.

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